

Notice of References Cited	Application/Control No. 09/530,553	Applicant(s)/Patent Under Reexamination DEBOY ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Omura et al., "A breakdown voltage simulator for semiconductor devices with depleted floating regions", NASECODE VI. Proc. 6th Intl. Conf. on Numerical Analysis of Semiconductor Devices and Integrated Circuits, Dublin, IRE, 11-14 July 1989, p.372-7
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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